20

محمد ابراهيم محمد عبد الحميد سيد
Sec 2

Question (1):

1 Address field Contain 20 where is operand ?

a) Immediate
* operand is part of Instruction and has value 20.

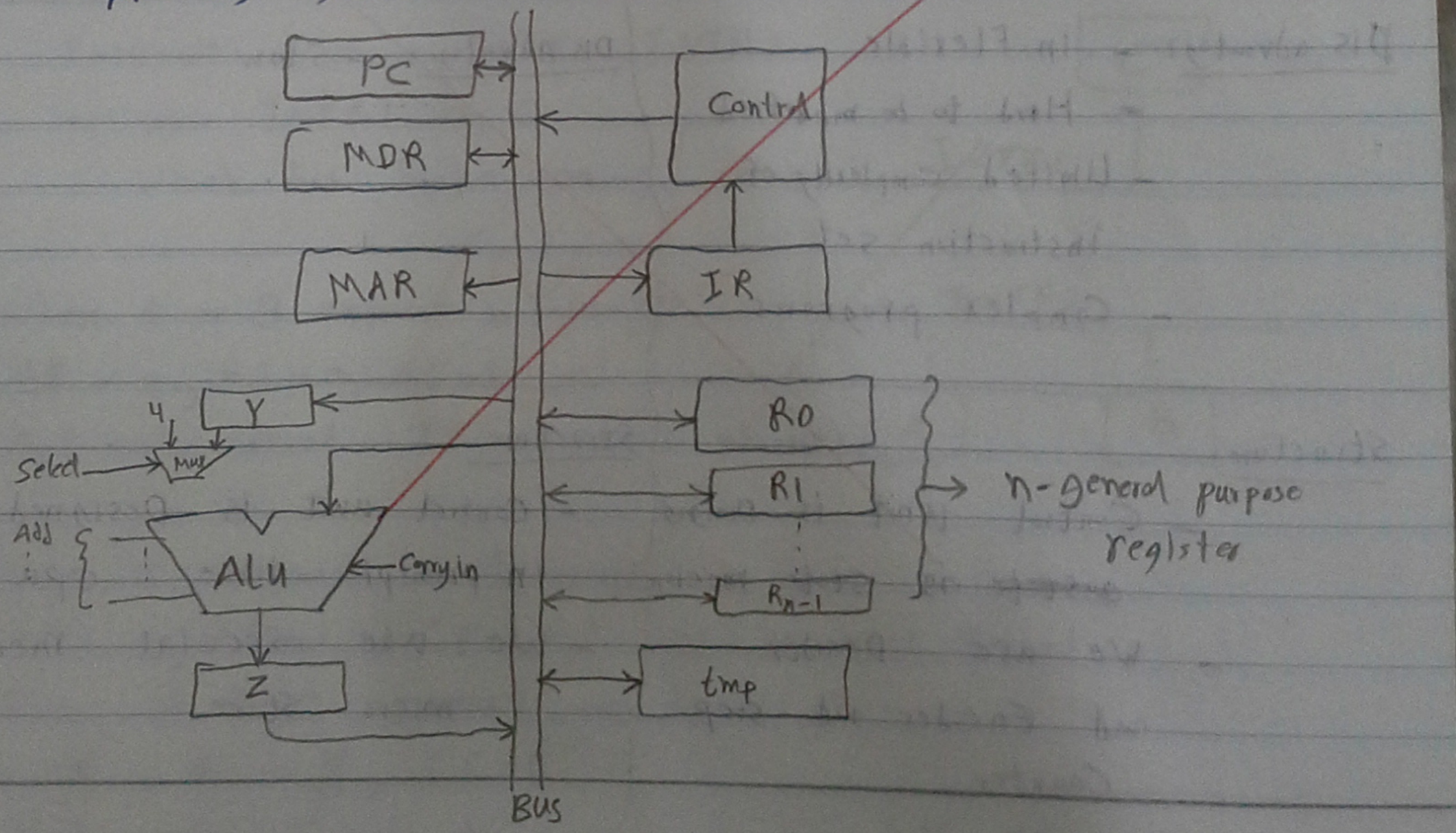
b) Direct
~~* operand location is the Contint of~~
* operand location is memory location 20

c) Indirect
* operand location is Content of memory location 20

d) Register
* operand location is register 20

e) Register Indirect
* operand location is content of register 20

2 Design datepath in single Bus orgnization
then Add LOC, R2, R3
Assuming Instruction with two word



Add Loc, R2, R3

1) PC_{out}, MAR_{in}, Select 4, Add, Read, Z_{in}
2) Z_{out}, PC_{in}, Y_{in}, WMFC
3) MDR_{out}, IR_{in}.
4) PC_{out}, MAR_{in}, Select 4, Add, Read, Z_{in}
5) Z_{out}, PC_{in}, Y_{in}, WMFC
6) MDR_{out}, MAR_{in}, Read
7) $R2_{out}$, Y_{in}, WMFC
8) MDR_{out}, Add, Select Y, Z_{in}
9) Z_{out}, $R3_{in}$, End

3

(3)

Hard wired

Advantage: Fast

Dis advantage:
- in Flexible
- Hard to be modified
- Limited complexity of instruction set
- Complex programs

Structure:
- Control unit is Design as State machine
- We use Decoder and Encoder and step Counter

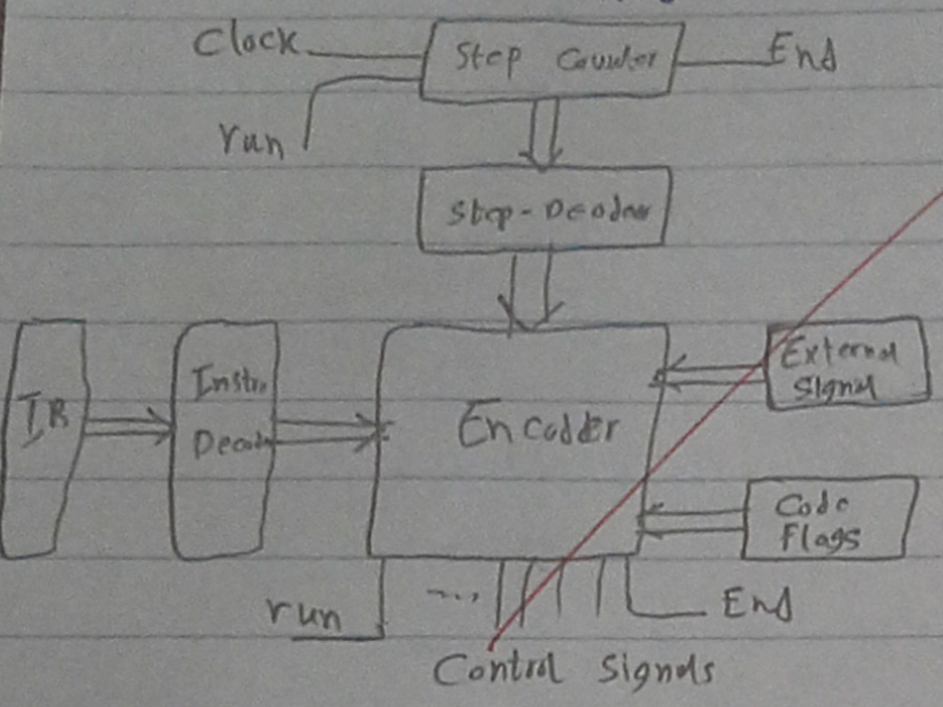
micro progremed

Advantage:
- Flexible
- Complex Instruction set
- easy program

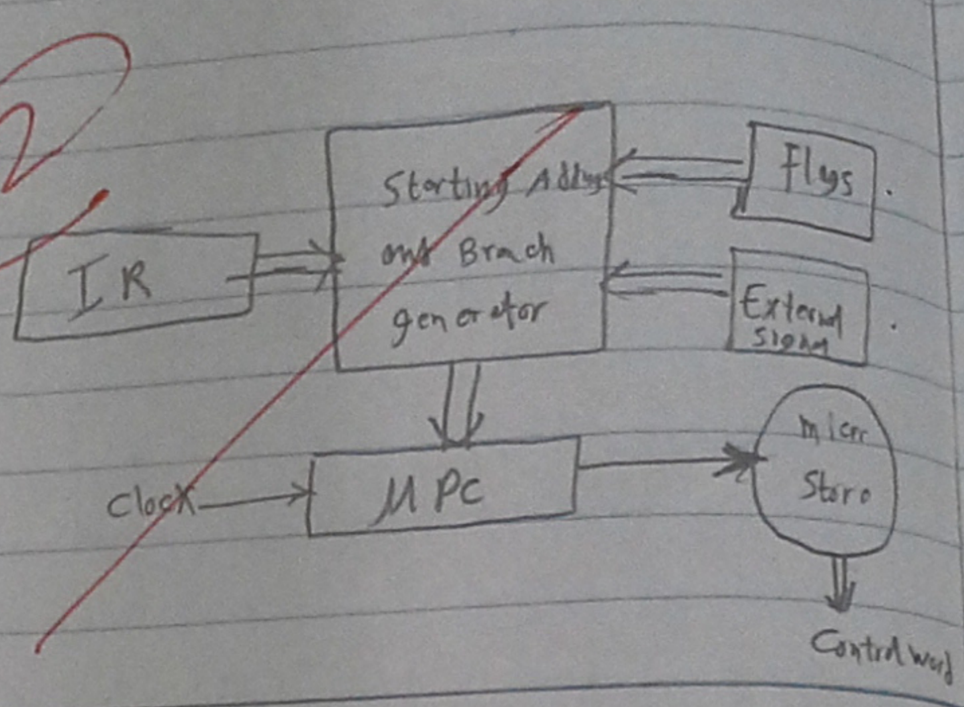
Dis Advantage:
- Slow

Structure
- Control unit is Designed hierrichaly in prenciple like cpu Design
- We use special memory called micro Store

~~buffer~~ hard wired



micro programmed



Add

1) PC_{out}, MA
2) ~~PCin~~ Z_{out}
3) MDR_{out},
4) PC_{out} ,
5) Z_{out} ; P
6) MDR_{out},
7) $R2_{out}$,
8) MDR_{out}
9) Z_{out} , R

Questirn (2):

[1] Piffrence between subroutine and Interrupt service routine ?

1- subroutine perform task required by calling program
2- Interrupt service routine may have no common thing with the Interrupted program
3- Interrupt service routine and program may belong to diffrent users
4- Sub routine is called by program
5- Interrupt service routine called by Interrupt request of I/o Device
6- Sub routine store only the content of pc
7- Interrupt service routine store pc and condition code flags and may store registers

[3] Hard wi

Advantage: Fast

Dis advantag: - i
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Structure:
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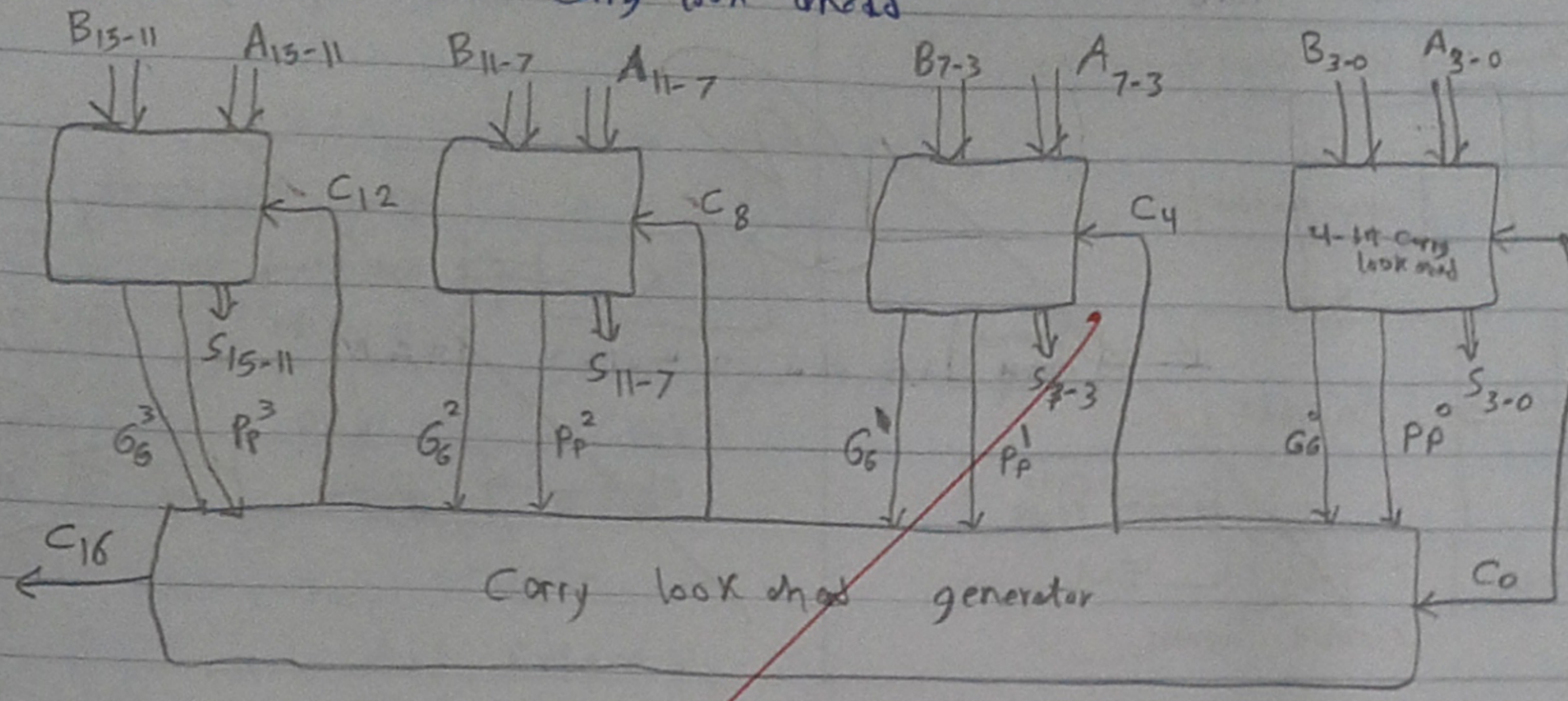
(2) Design 16 bit Carry look ahead



To build thith Circuit we need to 4 4-bit carry look ahead and Carry look ahead generator

$$C_{16} = G_6^3 + P_p^3 G_6^2 + P_p^3 P_p^2 G_6^1 + P_p^3 P_p^2 P_p^1 G_6^0 + P_p^3 P_p^2 P_p^1 P_p^0 C_0$$

D 1 1 4 1 1 → 5

C_{16} → 5 gates

C_{12} → 4 gates

C_8 → 3 gates

C_4 → 2 gates

Carry look ahead need 14 gate

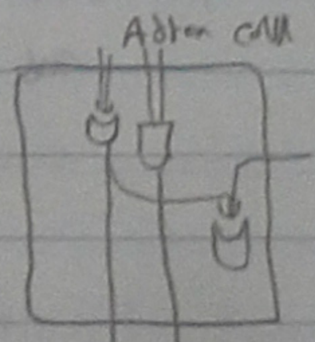
Inside 4-bit carry look ahead Adder Assuming that we don't generate C_1, C_2, C_{12}, C_{16}

Inside carry look ahead need 9 gates

we have 4 Inside carry look ahead

For each Cell we need 3 gates

we have 16 Cell



Inside Carry look ahead we need to generate G_6^*, P_p

So we need 4 gates For all G_6 and 1 gate For all P_p

Total gates = 14 + 4*9 + 16*3 + 4*4 + 1*4

= ~~118 gates~~

= 118 gates

Sec 2

Question (2)

(3) A, B, C Connected to bus

C → high perioty A, B → Same pesiorty (Low)

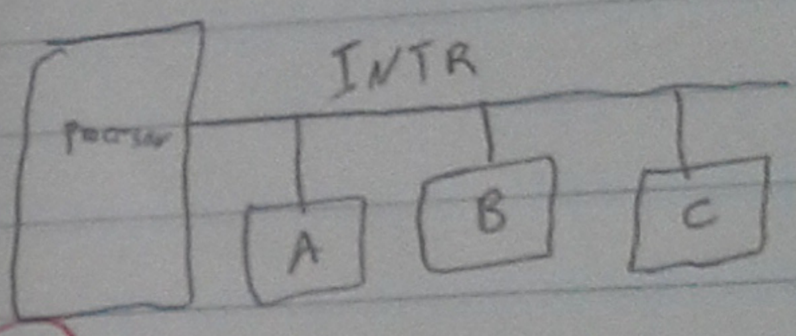
a) one Interrupt request Line

We use Interrupt Enable for that AE, BE, CE - Active High -

1- When A or B request an Interrupt
AE = 0 , BE = 0 , CE = 1

2- When C request an Interrupt
AE = 0 , BE = 0 , CE = 0

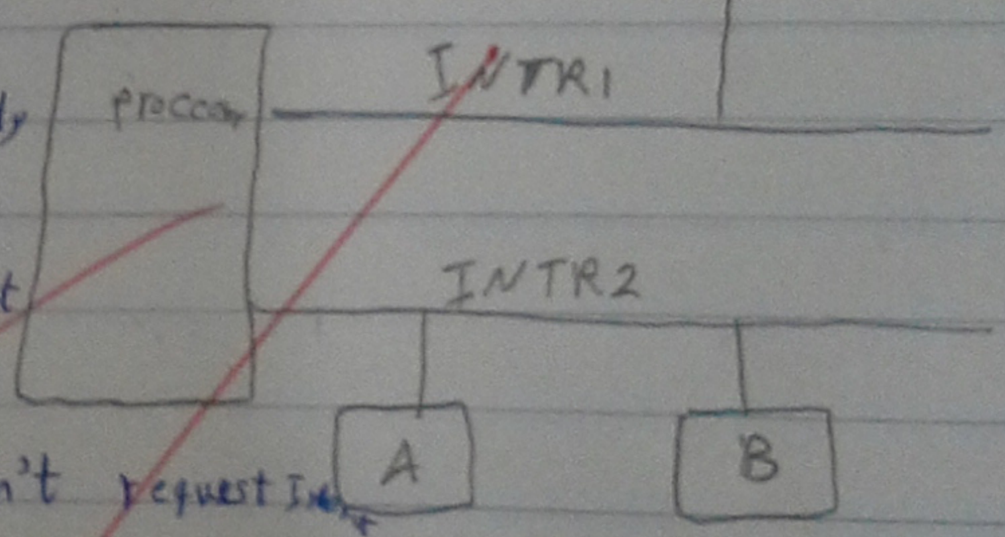
3- Defoult is that
AE = 1 , BE = 1 , CE = 1



~~We Could use also Interrupt Acoslage for that~~

~~We Could~~

b) Two Intterupt Line INTR1 , INTR2
we use INTR1 For C
which has higher periorty



1- When A or B request an Interrupt
AE = 0 , BE = 0, CE = 1
A, B will served If C don't request In

2- When C request an Interrupt
AE = 1 , BE = 1 , CE = 0 and C would Served

3- When A, B, C request an Interrupt
AE - X , BE = X , CE = 0
But only C will be served

AE = X → Don't Care